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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,007	08/31/2003	Wen-Chieh Wu	NTCP0013USA	2006

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,007	WU ET AL.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 31 August 2003. Claims 1-8 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Pan et al. (6,067,680).

Pan et al. disclose a method of manufacturing a semiconductor device including a conductive plug where a substrate (12) has a diffusion region (30) thereon; depositing a dielectric layer (32) on the substrate (12); forming an opening (34) in the dielectric layer (32), the opening (34) exposing a part of the diffusion region (3) of the substrate (12) (col. 3, lines 44-65); depositing a first non-doped silicon layer (36) in the opening (34) (col. 3, line 65 thru col. 4, line 3); in-situ depositing a first transient pure phosphor film on the first non-doped silicon layer (36) in the opening (34) (not shown), wherein the first non-doped phosphor atoms of the first transient pure phosphor film diffuse into the first non-doped silicon layer (36) in no time to form a first doped silicon layer (36a) (col. 4, lines 4-25; col. 5, lines 46-53); in-situ depositing a non-doped silicon layer (40) on the first doped silicon second layer (36a) in the opening (34) (col. 4, lines 25-35); in-situ

depositing a second transient pure phosphor film on the second non-doped silicon layer (40) in the opening (34) (not shown), wherein phosphor atoms of the second transient pure phosphor film diffuse into the second non-doped silicon layer (40) in no time to form a second doped silicon layer (40a) (col. 4, lines 36-47; col. 5, lines 46-53); and in-situ depositing a third non-doped silicon layer (60) on the second doped silicon layer (40a) in the opening (34), wherein the third non-doped silicon layer (60) fills the opening (34) (col. 5, lines 24-40).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan et al. in view of Ohshima (5,420,074).

Pan et al. disclose the subject matter claimed above except performing a chemical mechanical polishing (CMP) process to remove the silicon layers outside the opening, leaving the first doped silicon layer, the second doped silicon layer, and the third non-doped silicon layer in the opening to form a conductive plug; the diffusion region as a N+ diffusion region, and wherein the first and second transient pure phosphor films are both formed by CVD; and a first device, which is a layer of metal interconnection.

Ohshima discloses a method of manufacturing a semiconductor device including a conductive plug where a substrate (101) has a diffusion region (102) thereon, wherein the diffusion region (102) bas a N+ diffusion region; depositing a dielectric layer (103) on the substrate (101); forming an opening (105) in the dielectric layer (103), the opening (103) exposing a part of the diffusion region (102) of the substrate (101) (Fig. 2A; col. 3, lines 46-55); depositing a first non-doped silicon layer (106) in the opening (105) (Fig. 2B; col. 3, lines 56-66); in-situ depositing a first transient pure dopant film (107l) on the first non-doped silicon layer (106) in the opening (105) (Fig. 2B), wherein the first non-doped dopant atoms of the first transient pure dopant film (107l) diffuse into the first non-doped silicon layer (106) in no time to form a first doped silicon layer (106) (Fig. 6A; col. 4, lines 47-51; col. 6, lines 41-50); in-situ depositing a non-doped silicon layer (108) on the first doped silicon second layer (106) in the opening (105) (col. 4, lines 21-34); in-situ depositing a second transient pure dopant film (109l) on the second non-doped silicon layer (108) in the opening (105) (Fig.2D), wherein dopant atoms of the second transient pure dopant film (109l) diffuse into the second non-doped silicon layer (108) in no time to form a second doped silicon layer (108) (Fig. 6B; col. 4, lines 47051; col. 6, lines 51-61); in-situ depositing a third non-doped silicon layer (110) on the second doped silicon layer (108) in the opening (105), wherein the third non-doped silicon layer (110) fills the opening (105) (Fig. 2F; col. 4, lines 43-46); and performing a chemical mechanical polishing (CMP) process to remove the silicon layers outside the opening (105), leaving the first doped silicon layer (106), the second doped silicon layer

(108), and the third non-doped silicon layer (110) in the opening (105) to form a conductive plug (113) (col. 4, line 63 thru col. 5, line 12).

Ohshima further discloses forming the first and second transient pure dopant films (107I/109I) by CVD (col. 4, lines 21-34). Ohshima also discloses forming the conductive plug on a first device (115), which is a layer of metal interconnection (Fig. 4; col. 5, lines 46-62). Ohshima disclose that the dopant may be phosphor (col. 4, lines 24, 25).

Since Pan et al. and Ohshima are both from the same field of endeavor, a method of manufacturing a semiconductor device including a conductive plug, the purpose disclosed by Ohshima would have been recognized in the pertinent art of Pan et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Pan et al. by performing a chemical mechanical polishing (CMP) process to remove the silicon layers outside the opening, leaving the first doped silicon layer, the second doped silicon layer, and the third non-doped silicon layer in the opening to form a conductive plug; the diffusion region as a N+ diffusion region, and wherein the first and second transient pure phosphor films are both formed by CVD; and a first device is a layer of metal interconnection as taught by Ohshima to lower contact resistance (col. 2, lines 28-44).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pan et al. in view of Ohshima and Dreybrodt et al. (6,479,373).

Pan et al. in view of Ohshima disclose the subject matter claimed above except situating the semiconductor substrate in a CVD vacuum chamber; and alternately

introducing silane gas and phosphine gas into the CVD vacuum chamber and undergoing a chemical vapor deposition reaction to deposit a plurality of pure silicon layers and pure phosphor films, wherein each of the pure phosphor films is interposed between two of the pure silicon layers, and phosphor atoms of the pure phosphor films diffuse into adjoining pure silicon layers.

Dreybrodt et al. disclose a method of manufacturing a semiconductor device where a semiconductor substrate has a dielectric layer thereon; situating the semiconductor substrate in a CVD vacuum chamber (col. 10, lines 14-16); and alternately introducing silane gas and phosphine gas into the CVD vacuum chamber and undergoing a chemical vapor deposition reaction to deposit a plurality of pure silicon layers and pure phosphor films, wherein each of the pure phosphor films is interposed between two of the pure silicon layers, and phosphor atoms of the pure phosphor films diffuse into adjoining pure silicon layers (col. 9, line 55 thru col. 10, line 12).

Since Pan et al. and Dreybrodt et al. are both from the same field of endeavor, a method of manufacturing a semiconductor device, the purpose disclosed by Dreybrodt et al. would have been recognized in the pertinent art of Pan et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Pan et al. by situating the semiconductor substrate in a CVD vacuum chamber; and alternately introducing silane gas and phosphine gas into the CVD vacuum chamber and undergoing a chemical vapor deposition reaction to deposit a plurality of pure silicon layers and pure phosphor films, wherein each of the pure phosphor films is

interposed between two of the pure silicon layers, and phosphor atoms of the pure phosphor films diffuse into adjoining pure silicon layers as taught by Dreybrodt et al. to avoid undercutting in subsequent processing steps (col. 2, lines 4-33).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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